REMARKS

Reconsideration of the above-indicated patent application, as amended, is respectfully requested. The present amendment is responsive to the Office Action mailed February 12, 2004. Claims 1-15 have been rejected. Accordingly, amended claims and supporting remarks are hereby presented that particularly point out and distinctly claim the subject matter that applicant regards as the invention. No new matter has been added.

DRAWING OBJECTIONS

In the drawing objection, the Examiner has stated that "some drawings contain material that is illegible." However, there is no Draftsperson's Drawing Review (PTO-948) attached to the Action. Further, the Examiner has not indicated which drawings(s) and elements thereof are taken to be illegible. Therefore, Applicant has not been given sufficient information so as to comply with this requirement. It should be noted that Applicant is still permitted to submit informal drawings in accordance with Rule 85. Therefore, it is respectfully submitted that the informal drawings are suitable for Examination purposes at least until such as time as the Examiner explicitly points out the alleged objectionable material. A supplemental copy of the informal drawings is hereby submitted herewith.

THE INVENTION

As described in detail in the present specification, the present invention is directed to a microcode controller system including: a microcode controller for generating control signals and decoding address data. A level-sensitive address latch is provided for storing address data

decoded by the microcode controller. The address latch opens during either a high-level state or a low-level state of a clock cycle to store said decoded address data therein. A level-sensitive code word latch is provided for storing code word data. The code word latch closes during the other of the high-level or low-level states clock cycle, simultaneous with the opening of the address latch. A microcode memory is provided, wherein code word data is read out of the microcode memory in response to presentation thereto of the address data stored in the address latch. The code word latch opens during the subsequent portion of the clock cycle to store the code word data read out from the microcode memory. The address latch simultaneously closes in the same state of the clock cycle. The microcode controller generates control signals and decodes at least one address, using the code word data stored in the code word latch. An advantage of this approach is that the current code word can be frozen at mid cycle so it can be used for crypto operations during the second half of the clock cycle. Simultaneously, the fetch (read) of the next code word can take place in second half of the clock cycle (rather than waiting for the next clock edge) based on the address which flows through the open address latch. In this way the next code word can be accessed more earlier resulting in a faster clock cycle as illustrated in Figure 4 of the current invention.

It should especially be appreciated that the preset latches are components that respond to the state of the square-wave signal, either high or low. This distinction is very important since latches do not respond to rising and falling edge effects, as implied by the Examiner. Also, latches are in fact different from registers, contrary to the statement by the Examiner. By providing an address latch that responds to a clock signal level and a code word latch that responds to the respective other clock signal level, it is possible to read a microcode

address of a code word while the code word of the previous cycle is also being read out. In this way, the present system performs "cycle stealing" in that subsequent operations on two sequential code words may be performed simultaneously in the microcode controller system, during the same clock cycle. This is a dramatic improvement over previous-type systems in which subsequent operations on the same code word would be performed in sequential clock cycles. In this way, the present system greatly accelerates the generation of control signals in the microcode controller. This has special applicability to encryption/decryption operations performed with RC4, as is disclosed at present. In any case, the present system is very different from the prior art at issue.

THE REJECTIONS UNDER 35 U.S.C § 103

Claims 1-12 had been rejected under Section 103 as being unpatentable over Matthews, Jr. (i.e. "Matthews"), U.S. Pat. No. 6,549,622 in view of Pancholy et al., U.S. Pat. No., 6,292,403. This rejection is respectfully traversed, particularly as applied to the amended claims. The Examiner states:

> "The office interprets the applicant claims to read as follows. A recurring cycle that involves read/write functions from and to a controller and a memory device in one clock cycle."

This is a misreading of the claims. There in no discussion in the claims of "read/write functions." In fact, it is clear from the claims that only read and execute functions are performed. In fact, it is clear from the claims that in a first part of a clock cycle, a latch appears so that a code word is read out; in a second part of the clock cycle, another latch opens to decode the code word. In this way, it is clear that operations are performed on different code words

within the same clock cycle. The present system is thus a high-speed, efficient "pipelining" system.

The Examiner further states:

> "It is known to one ordinarily skilled in the art that a clock cycle has a rising edge and a falling edge. Applicant does not specify which events are triggered by the rising edge and which events are triggered by the falling edge. Applicant's invention comprises 2 latches also known as registers in the art. When reading and writing to the registers, the applicant uses the terms "open" and "close" to refer to enabling the reading and writing to the registers."

The Examiner is mistaken on many points in this passage, and thus, the claims are misread in several respects. The claims have recited "latches." At present, the claims have been amended to recite "level-sensitive latches." The Examiner should note that these terms are well known in the art as components that respond to the level of a square-wave clock signal, i.e. either high or low. Thus, they are not triggered by edge-effects as alleged by the Examiner. Further, a latch is not equivalent to a register, as alleged by the Examiner, and has a specific, distinct meaning and connotation in the art. Thus, it is not proper to equate the opening and closing of the latches with the simple reading and writing to register.

Further to the above, the Examiner proceeds to apply the Matthews reference to the claims. Matthews is directed to a system and method for fast hardware implementation of the RC4. Matthews does not disclose a microcode controller as with the present system, but instead discloses a control logic implementation very different in structure and operation to that of the present system. The Examiner cites excerpts from Matthews taken to read onto the present claims. For example, the Examiner cites col. 2, line 59 as allegedly disclosing the reduction of cycles needed for encryption/decryption. Col. 4, line 48 is cited as reducing cycles from 6 to 2.

It is noted that these excerpts are simple statement of intended use. They do not include any actual discussion of structure that could accomplish those functions. The other cited portions simply list elements disclosed by Matthews, presumably taken to read on the references. However, in no respect is anything cited in Matthews to satisfy the claim requirements of a microcode controller having level-sensitive latches that perform various read and decode operations with "cycle stealing" in response to respective high and low levels of a clock cycle. It is respectfully submitted that for the reasons given above, Matthews is entirely unsuitable as applied to the presently claimed system.

The Examiner admits that Matthews is deficient in disclosing a "read/write process...executed during one clock cycle." For this purpose, the Examiner brings in Pancholy et al. This reference discloses a circuit and method for single-cycle read/write operations. As seen from the timing diagram of Fig. 4 of Pancholy et al., and the corresponding structure shown e.g. at Fig. 3, Parcholy et al. simply uses circuitry to create a faster clock, with a read and write operation performed in the same cycle. There is no way that Pancholy et al. can be construed as performing two read operations (next word microcode fetch and read of SBOX during execution of microcode word) in the same cycle, as with the present system. Thus, Pancholy et al. cannot perform "cycle stealing," nor can it pipeline processing operations, as with the present system.

In any event, there is nothing in Pancholy et al. to shore up the deficiencies of Matthews. Therefore, even if this proposed combination could be deemed proper, it would still fall to satisfy the requirements of the claims, i.e. reciting a "cycle stealing" microcode controller incorporating address and code word latches in accordance with the amended claims. Reconsideration and withdrawal of this rejection is respectfully requested.

Claims 13-15 had been rejected under Section 103 as being unpatentable over Matthews in view of Rogers et al. U.S. Pat. No. 5,517,657. This rejection is also respectfully traversed.

This rejection is also based on the same misreading of the claims as with the previous rejection. Also, the same arguments are repeated with respect to the Matthews reference. Hence, the arguments from above that respond to these issues are reiterated, for the purpose of this grounds of rejection. The Examiner brings in Rodgers et al. to shore up the deficiencies of Matthews. However, Rodgers is only cited for incidental teachings, the Examiner admits that Rodgers et al. is not directed to a microcode controller. The holding of obviousness is based on a citation of "boilerplate" broadening language from the reference, a vague allusion to non-disclosed embodiments, lacking any specific teaching or structure. In any case, it is clear that the thin disclosure of Rodgers et al. cannot be relied upon to satisfy the requirements of the claims, i.e. "level-sensitive latches" that read out and process code words go to provide a "cycle stealing" microcode controller. Thus, even if a combination with Matthews could be considered proper, such a combination would still fail to satisfy the requirements of the claims. Reconsiderations and withdrawal of these grounds of rejection is respectfully requested.

In view of the foregoing it is respectfully submitted that the present claims, as currently amended, distinguish over the prior art. A notice to that effect is earnestly solicited. If the Examiner believes there are any further matters, which need to be discussed in order to expedite the prosecution of the present application, the Examiner is invited to contact the undersigned.

Respectfully submitted,
TUCKER ELLIS & WEST LLP

Jay P. Ryan
Agent for Applicant
(Registration No. 37,064)
1150 Huntington Building
925 Euclid Avenue
Cleveland, Ohio 44115-1475
Customer No. 23380
216-696-4396 (phone)
216-592-5009 (fax)